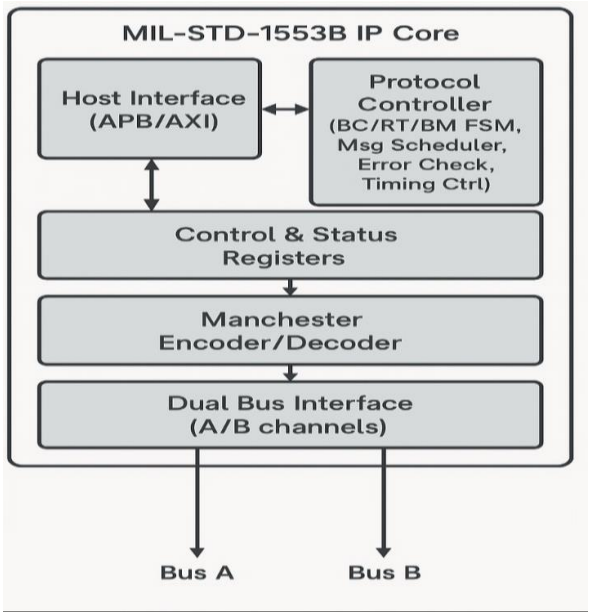
DESIGN IP DATASHEET

MIL-STD-1553B BRT

The silicon proven **MIL-STD-1553B IP Core** delivers robust, field-proven digital communication for mission-critical avionics, defense, and industrial control systems. Supporting fully configurable operation as a **Bus Controller (BC)**, **Remote Terminal (RT)**, or **Bus Monitor (BM)**, this IP core enables seamless integration of the MIL-STD-1553B dual-redundant serial protocol into any SoC or FPGA platform.

Engineered for reliability and strict compliance, the core supports all protocol timing and electrical requirements, including error checking, status reporting, and message scheduling. The architecture is highly configurable, allowing for single or multiple RT instantiations, advanced command/data scheduling, and custom status monitoring. APB/AXI host interfaces ensure easy connection to a wide range of bus fabrics.

Ideal for: Avionics data buses (flight control, mission computers), Satellite & space systems, Defense/ground vehicle communications, Industrial and transport control systems.



Features

- Full compliance with MIL-STD-1553B/1553A protocol
- Configurable operating mode: Bus Controller (BC), Remote Terminal (RT), Bus Monitor (BM)
- Dual-redundant bus support (A/B channel failover, automatic switchover)
- Manchester II bi-phase encoding/decoding
- 32/16-bit parallel or streaming CPU interface (APB/AXI4-Lite options)
- Programmable message scheduling table and interrupt controller (BC mode)
- Automatic command/response sequence handling (RT mode)
- Comprehensive error detection: parity, sync, format, timing, gap errors
- Programmable status word, subaddress, and message validation
- Integrated transmit/receive FIFOs and DMA support
- Built-in self-test and loopback modes

Deliverables

- Synthesizable RTL test bench, simulation scripts, and full documentation