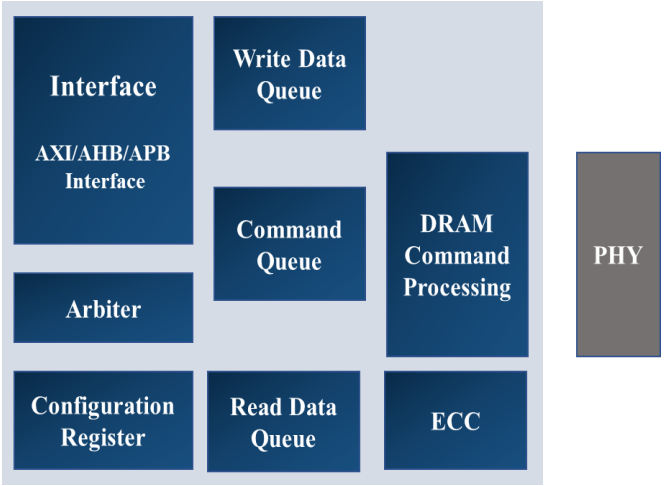
DESIGN IP DATASHEET

DDR Controller

These DDR controllers encompass two essential elements: the DDR Protocol and Memory Controller. They are engineered to provide comprehensive support for a range of JEDEC DDR standards, including DDR3, DDR2, Mobile DDR and SDRAM. Accessibility to all controller registers is made seamless through industry-standard APB and AXI buses, complemented by built-in self-test capabilities. Offering a spectrum of programmable parameters, they can be effortlessly reconfigured to operate in different modes.

The Controller IP is meticulously developed and validated to mitigate risks for the customer, ensuring the success of their System-on-Chip (SoC) designs from the outset. Aligned with PHY IP on advanced semiconductor process nodes, it boasts robustness under varying traffic loads and interoperability with memory chips from diverse suppliers. Additionally Fault tolerant feature is also available with the core in FT versions of the same.



Benefits

- Conforms to JEDEC-standard DDR2 and DDR protocols (JESD79-2 and JSED79)
- Silicon Proven
- Programmable timing parameters to support components from various vendors, ensuring broad compatibility

Features

- ➔ Provides separate ports for host CSR and host DATA access configurable for FIFO, APB, AHB, or AXI interfaces
- ➔ Fully pipelined command, read and write data interfaces to the memory controller.
- ➔ Advanced bank look-ahead features for high memory throughput.
- ➔ Front-end interface to 8 standard AXI ports.
- ➔ A programmable register interface to control memory parameters and protocols including auto pre-charge.
- ➔ Full initialization of memory on memory controller reset.
- ➔ Built-in Self-Test (BIST) for external DRAM memories.
- ➔ Programmable memory data path size of full memory data width or half memory data width.
- ➔ Back-end interface to a DFI 2.1-Compliant PHY.
- ➔ Adheres to JEDEC-standard DDR3, DDR2 and DDR protocols (JESD79-2 and JESD79), ensuring compatibility and reliability.
- ➔ Features a configurable multi-port arbiter accommodating up to 32 host ports utilizing Host Memory Interface (HMI) or AMBA 3 AXI.
- ➔ Includes a programmable ultra-high priority port (port 0), typically designated for CPU use.
- ➔ Provides a separate configuration port using Controller Register Interface (CRI) or AMBA 3 AXI, with independent clocking for enhanced flexibility.
- ➔ Implements command re-ordering and scheduling strategies to optimize memory bus utilization.
- ➔ Enables command reordering between banks based on bank status, enhancing efficiency.
- ➔ Incorporates programmable priority arbitration and anti-starvation mechanisms to ensure fair access to memory resources.
- ➔ Offers configurable per-command priority with up to eight priority levels, serving also as per-port priority management.
- ➔ Automates scheduling of activate and pre-charge commands, as well as refresh operations, streamlining memory management.
- ➔ Supports memory interfaces ranging from 8 to 64 bits in 8-bit increments (expandable up to 72 bits with ECC).

- ➔ Facilitates programmable ECC generation, checking, and correction, enhancing data integrity.
- ➔ Accommodates up to four external memory ranks, providing scalability and flexibility.
- ➔ Integrates basic data training logic for compatibility with Synopsys DDR2/DDR PHYs, simplifying setup.
- ➔ Features automated Read DQS recognition with Dynamic Drift Compensation for optimized performance.
- ➔ Offers programmable timing parameters to support DDR2/gDDR2/DDR/gDDR SDRAM components from various vendors, ensuring broad compatibility.

Deliverables

- ➔ Synthesizable RTL design in Verilog
- ➔ Easy-to-use UVM based verification environment
- ➔ Synthesis & Verification Scripts
- ➔ Technical documents