

DESIGN IP PRODUCT SHEET



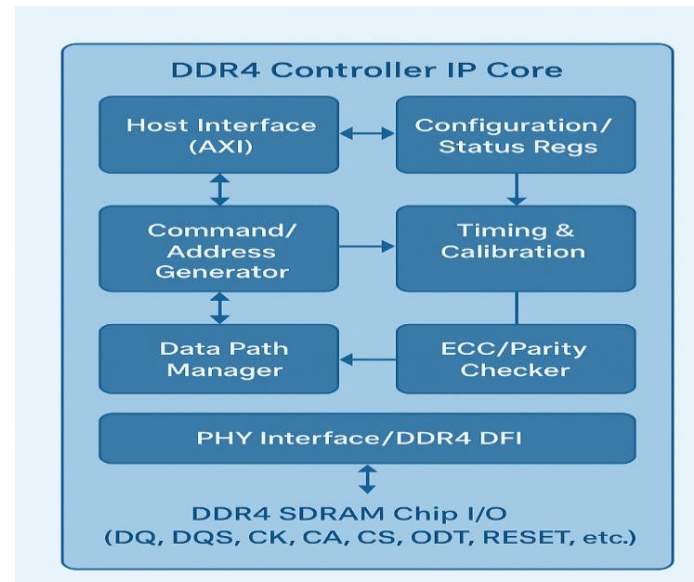
DDR 4 Controller

The **DDR4 Controller IP Core** is a high-speed, silicon-proven memory interface solution, fully compliant with JEDEC DDR4 SDRAM standards. Designed for seamless integration into FPGA, ASIC, and SoC platforms, the core supports data rates up to 3200 MT/s and advanced features such as multi-port arbitration, ECC, and low-power operation. With flexible APB and AXI host interfaces, the controller enables rapid, robust connectivity to high-density DDR4 memory devices for demanding embedded, consumer, and enterprise applications. Its architecture features multi-port arbitration, allowing simultaneous access from multiple system masters without bottlenecks, and built-in **Error Correction Code (ECC)** capabilities for enhanced data integrity and system reliability. This versatility makes it the ideal choice for designers seeking to maximize memory bandwidth, minimize latency, and ensure long-term reliability in mission-critical embedded, consumer, and enterprise platforms.

Ideal for: High-performance embedded processors, Network switches, routers, and storage controllers, Consumer multimedia and gaming devices, Industrial and automotive computing, AI/ML accelerators, HPC, and datacenter

Deliverables

Synthesizable RTL (Verilog/VHDL),
Comprehensive testbench (UVM)
Integration and synthesis scripts
Documentation (user guide, register map)
and Reference designs



Features

- Full JEDEC DDR4 SDRAM compliance (**up to 3200 MT/s**)
- Supports x4, x8, and x16 DDR4 DRAM devices
- Multi-port AXI/AXI4/AXI4-Lite interface (**optional APB for configuration**)
- 32/64/128-bit memory bus width options
- Automatic initialization, calibration, and training (write leveling, read gate)
- Configurable command, address, and data mapping
- Built-in Error Correction Code (ECC) and data scrub support
- Multi-bank, multi-rank, and multi-chip select support
- Low-power operation: **deep power-down, self-refresh, clock gating**
- Configurable burst length and programmable timing parameters
- Integrated FIFO and programmable arbitration for high throughput
- Comprehensive interrupt, error status, and debug features