DESIGN IP DATASHEET

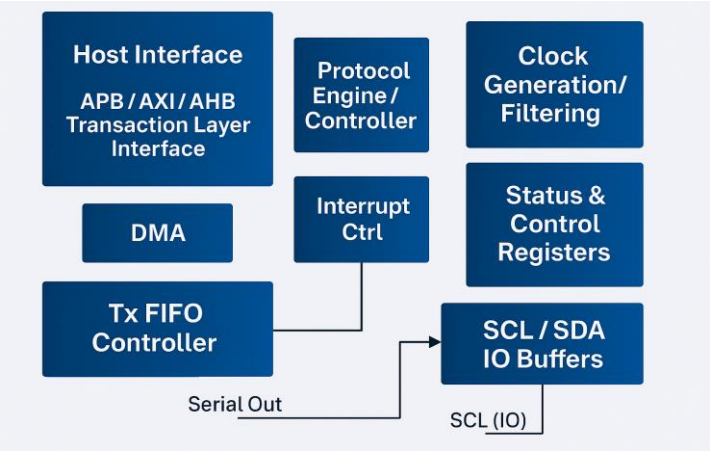
I2C Controller

The **I²C Controller IP Core** is a silicon-proven, highly reliable solution designed for robust synchronous serial communication in advanced SoC and FPGA platforms. Fully compliant with the latest I²C specifications, this controller enables seamless, industry-standard connectivity for a broad ecosystem of I²C-compatible devices—ranging from sensors and memory modules to power management ICs and peripheral controllers.

This IP core supports both **multi-master and multi-slave operation**, making it ideal for complex system topologies where flexibility and reliability are paramount. Its architecture is highly configurable, allowing design teams to tailor features such as FIFO depth, clock prescalers, interrupt management, and address modes (7-bit/10-bit) to specific application requirements.

With support for **APB and AXI host interfaces**, the core integrates easily into both legacy and modern SoC buses, ensuring rapid design closure and minimal integration effort. Advanced I²C protocol features—including clock stretching, multi-master arbitration, programmable SCL/SDA timing, and glitch filtering—are natively supported to maximize interoperability and data integrity, even in electrically noisy or demanding environments.

The core has been validated in silicon, guaranteeing proven performance, interoperability, and long-term reliability. Built-in error detection,



comprehensive status reporting, and integrated interrupt controller further streamline embedded software development and system debug.

Ideal for: embedded control, sensor hubs, mobile devices, industrial automation, power management, and any design standards-compliant I²C communication.

Features

- Fully compliant with I²C-Bus Specification Rev. 6.0
- Multi-master and multi-slave support
- Standard (100 kbps), Fast (400 kbps), and Fast-mode Plus (1 Mbps) speeds
- Clock stretching, arbitration, and programmable SCL timing
- 7-bit and 10-bit addressing
- Integrated interrupt controller
- Glitch filtering and bus error detection
- APB and AXI4-Lite slave interface options

Deliverables

- Synthesizable RTL(Verilog/VHDL), test bench, simulation scripts, and full documentation