DESIGN IP DATASHEET

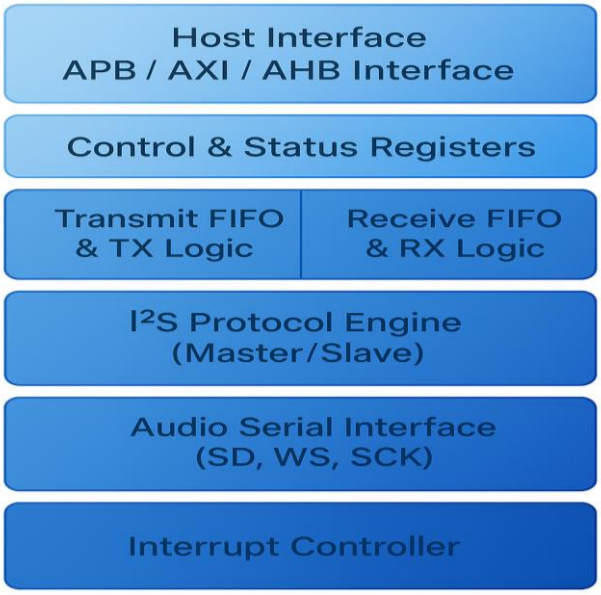
I2S Controller

With APB/AXI Interface - Audio Standards Compliant

The Silicon proven **I²S Controller IP Core** is a silicon-proven, feature-rich digital audio interface solution, engineered for reliable high-fidelity sound transmission in modern SoC and FPGA platforms. Designed to bridge processors with audio codecs, digital microphones, and other audio peripherals, it supports all popular serial audio standards—including industry-standard I²S, left-justified, right-justified, and time-division multiplexing (TDM) modes - enabling versatile integration into a wide range of multimedia and communication systems.

This IP core offers flexible word lengths, channel configurations, and programmable audio frame parameters, making it ideal for high-quality stereo, multi-channel, or multi-rate audio processing. Its architecture ensures low latency and robust clock domain crossing, supporting both master and slave operation to match your system topology.

With native APB and AXI host interface options, the I²S Controller IP Core delivers easy, configurable integration into both legacy and state-of-the-art SoCs, minimizing verification effort and reducing time-to-market. Built-in transmit and receive FIFOs, programmable clock generation, and comprehensive interrupt support ensure reliable data flow even under demanding real-time audio workloads.



Ideal for: embedded control, sensor hubs, mobile devices, industrial automation, power management, and any design standards-compliant I²C communication.

Features

- Fully compliant with I²S and PCM standards
- Master and slave operation Supports 8 to 32-bit word lengths
- Configurable data format (I²S, left-justified, right-justified, TDM)
- Multiple audio channels (stereo/mono, TDM)
- Programmable clock divider and frame sync
- Integrated FIFO for transmit/receive
- APB/AXI4-Lite interface

Deliverables

- Synthesizable RTL test bench, simulation scripts, and full documentation