DESIGN IP DATASHEET

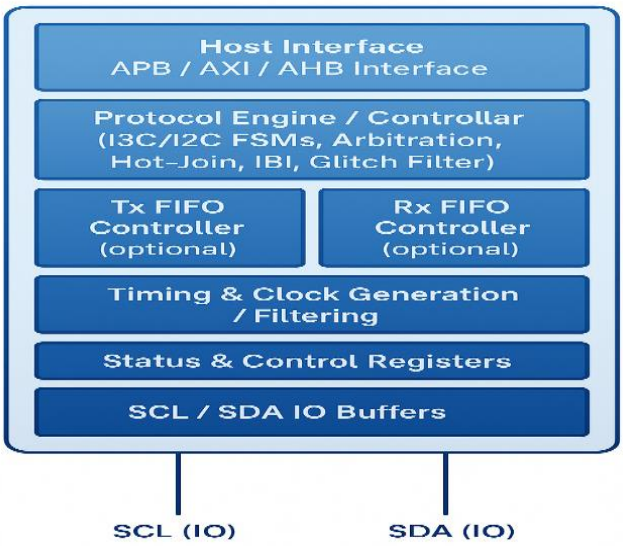
MIPI I³C Controller

With APB/AXI Interface – Backward Compatible with I²C

The **MIPI I³C Controller IP Core** is a high-performance, silicon-proven serial communication solution designed for next-generation embedded systems. Fully compliant with the MIPI Alliance I³C specification (v1.1 and beyond), this IP core supports both master and slave operation and offers seamless backward compatibility with legacy I²C devices on the same bus.

Designed for easy integration into SoCs and FPGAs, the core features configurable APB and AXI bus interfaces, low power consumption, and advanced features such as dynamic address assignment, in-band interrupt handling (IBI), hot-join capability, and support for high data rates. Its backward compatibility ensures interoperability in mixed I²C/I³C environments, enabling a smooth migration path from I²C to I³C technology.

Ideal for: embedded control, sensor hubs, mobile devices, industrial automation, power management, and any design standards-compliant I²C communication.



Deliverables

- Synthesizable RTL(Verilog/VHDL), test bench, simulation scripts, and full documentation

Features

- **MIPI I³C v1.1 compliant** (master and slave modes)
- **Full backward compatibility** with legacy I²C devices (multi-master and multi-slave support)
- **Data rates:** Standard up to 12.5 Mbps (HDR modes), legacy I²C rates (100/400/1000 kbps)
- **Dynamic address assignment** and static addressing for legacy I²C devices
- **In-Band Interrupt (IBI)** and Hot-Join support
- **Multi-controller (master) and multi-target (slave) capability**
- **Advanced power management:** Bus idle, sleep, wake, clock stretching
- **Programmable timing parameters** for SCL/SDA (clock stretching, glitch filtering)
- **Error detection:** Arbitration loss, parity, CRC, protocol violations
- **Integrated APB and AXI4-Lite slave interfaces**