DESIGN IP DATASHEET

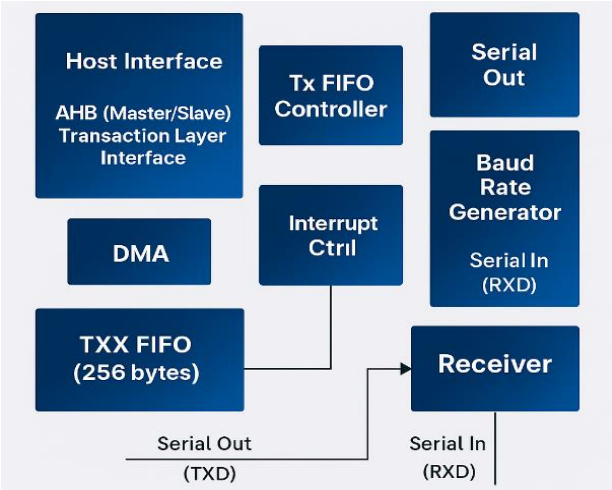
UART Controller with APB/AXI Host Interface

The **UART Controller IP Core** delivers high-performance, standards-compliant asynchronous serial communication for SoC and FPGA designs. Supporting APB and AXI bus interfaces, it ensures easy integration into modern and legacy systems.

Fully compatible with the 16550D UART protocol, the core features deep, programmable FIFOs, flexible data format control, and a wide baud rate range, enabling reliable operation in both low- and high-throughput applications. Comprehensive modem control and hardware/software handshaking (CTS, RTS, DSR, DCD, RI) provide robust interfacing with a broad range of peripherals.

Advanced interrupt support and thorough error detection (parity, framing, overrun, break) simplify software development and system reliability. All status and configuration are accessed through a familiar, intuitive register map. Deliverables include synthesizable RTL, test benches, and full documentation for rapid design-in and verification.

Ideal for: embedded processors, industrial control, serial debug, consumer electronics, and any design requiring reliable UART communication.



Features

- **Standards:** 100% compliant with UART 16550D/16750 and compatible with all industry UART protocols
- **Bus Interfaces:** Supports APB 2.0 and AXI4-Lite slave interface (selectable at synthesis time)
- **FIFO:** 256-byte transmit and receive FIFOs (programmable trigger levels, error recovery, timeout interrupts)
- **Data Width:** 5, 6, 7, or 8 bits per character
- **Stop Bits:** Configurable to 1, 1.5, or 2 stop bits
- **Parity:** Even, Odd, None, or Stick parity
- **Baud Rate Generator:** Programmable baud rates up to 1 Mbps (customizable up to clock/16)
- **Flow Control:** Hardware/software handshaking (CTS/RTS, DSR/DTR, DCD, RI support
- **Interrupts:** Comprehensive interrupt controller for transmit, receive, error, and modem events
- **Low Power:** Support for clock gating and low-power system integration
- **Synthesis:** RMM-compliant, optimized for ASIC and FPGA

Deliverables

- Synthesizable RTL(Verilog/VHDL), test bench, simulation scripts, and full documentation