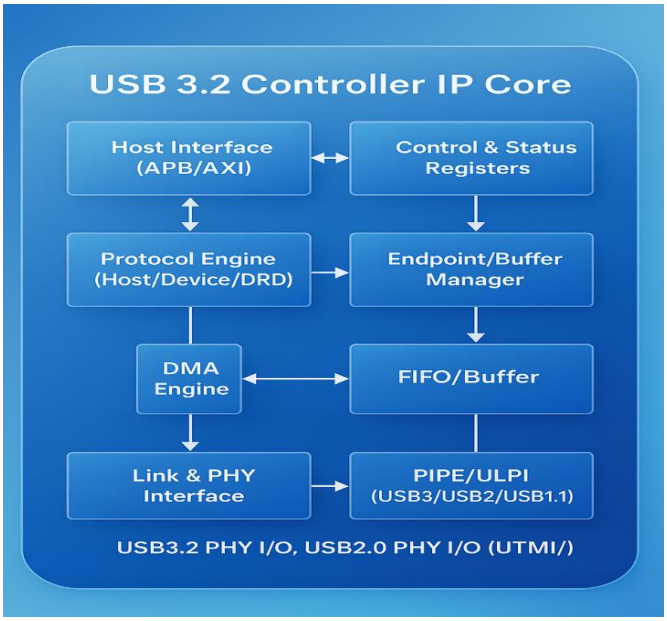
DESIGN IP PRODUCT SHEET

USB-3.2

The **USB 3.2 Controller IP Core** is a high-performance, silicon-proven solution enabling seamless SuperSpeed (5/10/20 Gbps), High-Speed (480 Mbps), and legacy USB communication for next-generation SoC, FPGA, and ASIC designs.
Compliant with the latest USB 3.2 specification, this core supports host, device, and dual-role operation, offering advanced power management, configurable endpoints, and robust error handling.
Available with standard APB/AXI interfaces, it accelerates system integration and shortens time-to-market for high-bandwidth, low-latency data transfer applications.



Ideal for: Smartphones, tablets, laptops, and high-performance embedded systems communications, Industrial and transport control systems, Data acquisition and streaming (video, audio, storage) Docking stations, hubs, and bridges, Automotive infotainment and diagnostics Industrial, medical, and test equipment

Deliverables

Synthesizable RTL (Verilog/VHDL), Comprehensive testbench (UVM) Integration and synthesis scripts Documentation (user guide, register map) and Reference designs

Features

- USB 3.2 Gen 1/2/2x2 SuperSpeed (5/10/20 Gbps) compliant
- Supports USB 2.0 (High/Full/Low Speed) and USB 1.1 legacy modes
- Host, Device, and Dual-Role (OTG) operation configurable
- Multi-lane operation (x1/x2) for SuperSpeed+ (10/20 Gbps)
- Backward compatible with USB 2.0/1.1 devices
- Configurable number of endpoints (up to 31 IN/OUT)
- Integrated DMA and endpoint FIFOs for high throughput
- Advanced power management: U0–U3 states, suspend/resume
- Native support for Isochronous, Bulk, Interrupt, and Control transfers
- Comprehensive error detection and recovery (CRC, EOP, protocol violation)
- USB Battery Charging, Link Power Management (LPM) support
- Standard APB/AXI4/AXI4-Lite host interface