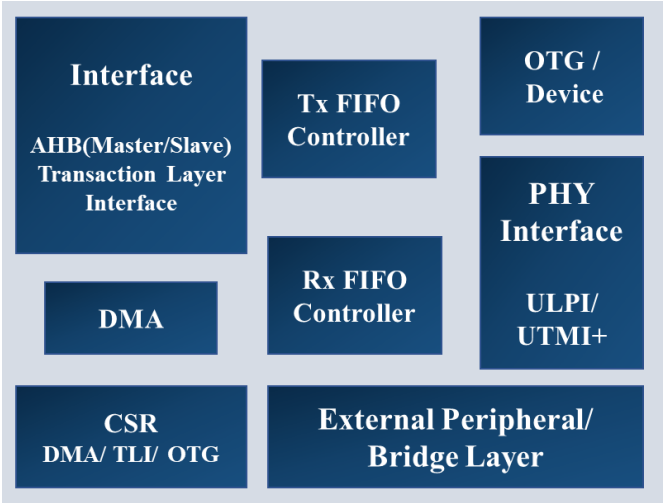
DESIGN IP DATASHEET

USB 2.0 OTG Controller

Crafted to adhere to the rigorous standards of the Universal Serial Bus Specification, Revision 2.0, along with the On-The-Go and Embedded Host Supplement, the VCores Design IP for USB 2.0 On-The-Go (OTG) Controller operates dynamically, seamlessly transitioning between Device and embedded Host roles. Its PHY interface complies with the UTMI and ULPI Specification.

This versatile Controller IP is meticulously engineered to effortlessly integrate into any System-on-Chip (SoC) architecture, catering to the ubiquitous nature of USB interfaces across consumer electronics, including smartphones, computers, and various other devices. It seamlessly interfaces with both VCores and third-party, UTMI-compliant PHYs. Furthermore, the controller's configuration and data interfaces align with industry-standard Arm® AMBA® AXI interfaces, ensuring compatibility and ease of integration.

Facilitating streamlined integration into target applications, the Controller IP comes equipped with a low-level driver.



Benefits

- Conforms to USB 2.0 specification, including USB 2.0 OTG and EH supplement
- Provides support for High-Speed (480Mbps), Full-Speed (12Mbps), and Low-Speed (1.5Mbps)
- Interfaces seamlessly with ULPI and UTMI+ for swift PHY integration

Supporting all available USB 2.0 classes, it boasts a proven track record in silicon and has undergone extensive validation across diverse hardware platforms.

Features

- ➔ Comprehensive support for USB 2.0 Speeds: Hi-Speed (480 Mbps), Full Speed (12 Mbps), and Low Speed (1.5 Mbps) specifications
- ➔ Versatile support for Hi-Speed OTG, Dual Role Device, Hi-Speed Host, and Hi-Speed Device functions tailored for low gate count and power-sensitive products
- ➔ Compatibility with both open-source and commercially available drivers to alleviate software engineering burden in target configurations
- ➔ Interfaces seamlessly with ULPI and UTMI+ for swift PHY integration
- ➔ Streamlined integration process for accelerated time-to-market
  Individual programmable burst size for Transmit and Receive DMA Engines
- ➔ The protocol layer operates all USB and OTG commands in hardware:
- ➔ Manages endpoint information through the endpoint info block
- ➔ Handles data exchange with UTMI+ PHY through parallel interface engines
- ➔ Allows for customization by removing OTG dynamic role-changing features, Host negotiation protocol, and session request protocol to optimize gate count
- ➔ Oversees downstream devices via the root hub
- ➔ Implements power-saving mechanisms by suspending and resuming controller operation according to USB specification power states
- ➔ Descriptor architecture allowing large blocks of data transfer with minimum CPU intervention & comprehensive status reporting for normal operation and transfers with errors
- ➔ Programmable interrupt options for different operational conditions
- ➔ Provides per-frame Transmit/Receive complete interrupt control
- ➔ Provides separate ports for host CSR and host DATA access configurable for FIFO, APB, AHB, or AXI interfaces

Deliverables

- ➔ Synthesizable RTL design in Verilog
- ➔ Easy-to-use UVM based verification environment
- ➔ Synthesis & Verification Scripts
- ➔ Technical documents