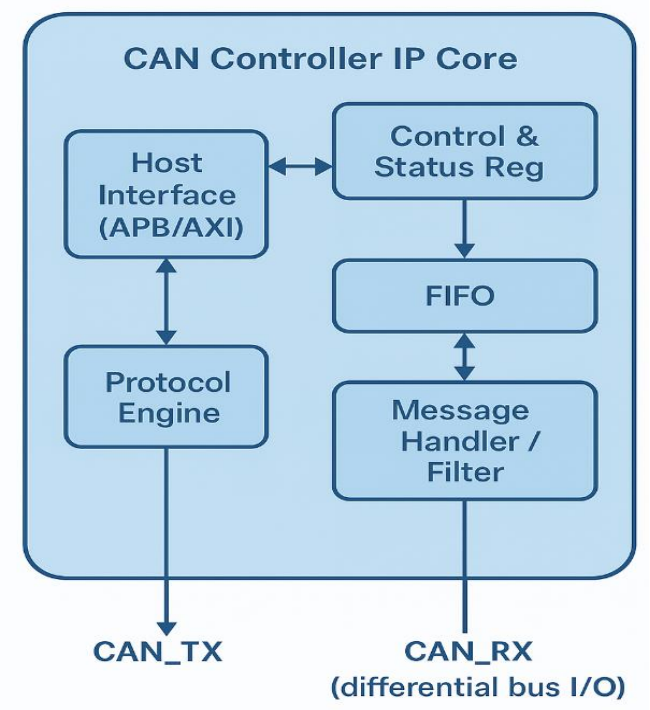
DESIGN IP PRODUCT BRIEF

CAN-Controller

The **CAN Controller IP Core** is a high-performance, silicon-proven solution for Controller Area Network (CAN) communication, fully compliant with the ISO 11898-1 standard. Supporting both Classical CAN (2.0A/B) and CAN FD, the core is designed for seamless integration into FPGA, ASIC, and SoC platforms. Flexible APB and AXI interfaces enable easy connection to a variety of bus architectures, making it ideal for automotive, industrial, and embedded applications. The core features advanced error handling, robust message filtering, and programmable acceptance masks to ensure reliable and secure data transmission even in noisy or mission-critical environments. Integrated transmit and receive FIFOs, hardware prioritization, and automatic retransmission maximize bus efficiency and minimize latency. Comprehensive interrupt support and detailed status reporting streamline software development and system diagnostics.

Ideal for: Automotive ECUs and gateways, Industrial automation and robotics, Medical devices and instrumentation, Smart energy and building control etc.



Deliverables

Synthesizable RTL (Verilog/VHDL), Comprehensive testbench (UVM) Integration and synthesis scripts Documentation (user guide, register map) and Reference designs

Features

- ISO 11898-1 compliant: Supports CAN 2.0A/B and CAN FD
- Bit rates: Up to 1 Mbps (Classical CAN), up to 8 Mbps (CAN FD)
- Configurable number of message objects/filters
- Flexible acceptance filtering and mask logic
- Supports standard (11-bit) and extended (29-bit) identifiers
- Transmit/receive FIFOs and hardware prioritization
- Automatic error detection, handling, and recovery
- Bus-off recovery and programmable time quanta
- APB and AXI host interface options
- Low power operation and wake-up detection