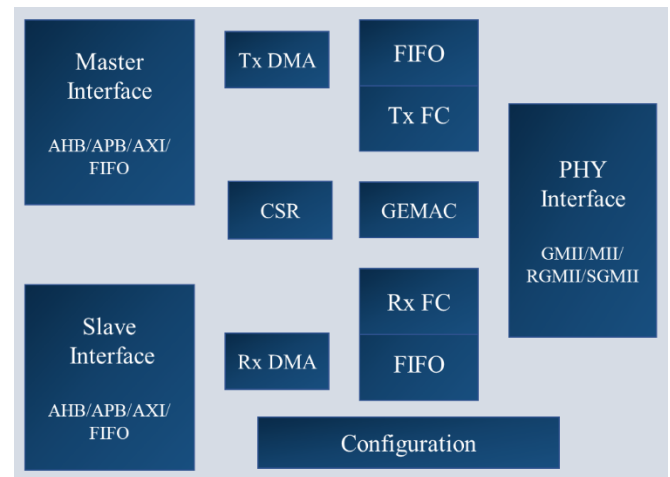


DESIGN IP DATASHEET



Ethernet MAC Tri-Mode 10/100/1000

The VCores Ethernet GMAC IP empowers hosts to transmit data using the Gigabit Ethernet protocol (IEEE 802.3) across speeds of 10M, 100M, and 1G. It comprises three primary layers: the Gigabit Ethernet Media Access Controller, the MAC Transaction Layer, and the MAC DMA Controller. The MAC Transaction Layer offers exceptional configurability, ensuring optimal performance and supporting a wide array of implementations tailored to end-system applications. Additionally, it provides extensive support for various application interfaces, facilitating seamless integration into SoCs. Leveraging silicon-proven technology and designed for straightforward integration into ASICs and FPGAs, the VCores GMAC IP boasts a user-friendly application interface, enabling designers to easily align functional and implementation goals with design requirements. Rigorously verified using cutting-edge methodologies, including



Benefits

- IEEE 802.3 and IEEE 1588-2008 Compliant
- Fully Configurable
- Silicon Proven

RTL design, verification, hardware verification and interoperability tests, this IP effectively mitigates risks.

Features

- IEEE 802.3 Compliant
- Support for IEEE 1588-2002 and IEEE 1588-2008 standards for precision networked clock
- Full-duplex mode at 10/100/1000 Mbps
- Half-duplex mode at 10/100 Mbps

- Configurable to support data transfer rates of 10/100/1000Mbps, 10/100 Mbps only or 1000 Mbps only
- Multiple TCP/IP offload functions supported
- PHY Interfaces
 - ◆ Gigabit Media Independent Interface (GMII)
 - ◆ Media Independent Interface (MII)
 - ◆ Reduced GMII (RGMII)
 - ◆ Serial GMII (SGMII)
- Fully synchronous design operating on a single system clock
- Supports:
 - ◆ 32/64/128-bit data transfers
 - ◆ Individual programmable burst size for Transmit and Receive DMA Engines
- Descriptor architecture allowing large blocks of data transfer with minimum CPU intervention & comprehensive status reporting for normal operation and transfers with errors
- Programmable interrupt options for different operational conditions
- Provides per-frame Transmit/Receive complete interrupt control
- Provides separate ports for host CSR and host DATA access configurable for FIFO, APB, AHB, or AXI interfaces
 - ◆ Start and stop modes
 - ◆ All AHB burst types

Deliverables

- Synthesizable RTL design in Verilog
- Easy-to-use UVM based verification environment
- Synthesis & Verification 1scripts
- Technical documents