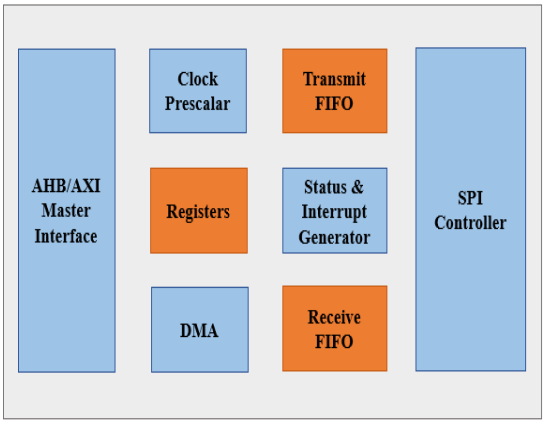
DESIGN IP DATASHEET

SPI Controller

The SPI – AHB bridge acts as a vital conduit, empowering an AHB host to seamlessly engage with a serial device at remarkable speeds via the SPI interface. Its utility extends across various applications such as flash memory cards and digital cameras. Both AHB and SPI interfaces offer versatile master and slave modes. The bridge facilitates efficient parallel-to-serial or serial-to-parallel conversions, achieving a maximum throughput of 50 Mbit/sec. To facilitate smooth data transfer between the AHB and SPI interfaces, sizable transmit and receive FIFOs (32-bit x 32-bit) are employed as data buffers. Additionally, the AHB master module incorporates a DMA controller, significantly enhancing system performance. Incorporated within the system is a SPI Clock Generator, offering flexibility with adjustable input clock frequencies to the SPI controller, ranging from 500 KHz to 50 MHz. The Status and Interrupt Generator play a pivotal role, furnishing essential data transaction insights to the AHB host processor, reflecting the states of FIFOs and DMA activities. The SPI controller itself comprises both a master and a slave component, programmable by the AHB host to support protocols such as TI,



Benefits

- Conforms to Various industry Specification.
- Silicon Proven
- Supports Full duplex Mode
- Maximum 50Mbit/Sec data

Furthermore, it operates in full SPI Motorola, or National SPI protocols.
duplex mode, ensuring seamless bidirectional communication. The Vcore High-Speed SPI–AHB IP Core encapsulates these functionalities, providing a robust foundation for efficient data exchange within the system, it boasts robustness under varying traffic loads and interoperability with memory chips from diverse suppliers. Additionally Fault tolerant feature is also available with the core in FT versions of the same.

Features

- ➔ Supplied as human readable VHDL source code
- ➔ Complies with Motorola, TI, and National SPI specifications, ensuring compatibility with various devices and protocols
- ➔ Supports both SPI master and SPI slave operations, accommodating diverse system architectures
- ➔ Maximum data throughput of 50 Mbit/sec, catering to data-intensive applications
- ➔ Allows pre-scaling for programmable clock rates ranging from 500 KHz to 50 MHz, enhancing flexibility and compatibility with different clocking schemes
- ➔ Supports full-duplex mode, enabling seamless bidirectional communication for enhanced versatility
- ➔ Developed in accordance with the AMBA revision 2.0 specification
- ➔ Facilitates AHB bus operation across a dynamic frequency range spanning from 1 MHz to 100 MHz
- ➔ Employs Bus master DMA modes for efficient data handling
- ➔ Offers support for both AHB master and AHB slave modes, ensuring versatility in system configurations
- ➔ Includes interrupt support, enhancing system responsiveness and management
- ➔ Features 32 x 32 bytes transmit and receive FIFOs, optimizing AHB - SPI data transfers for high performance
- ➔ RTL design in Verilog enables implementation as an SPI – AHB controller on ASICs or FPGAs
- ➔ The widely adopted Arasan High-Speed SPI – AHB IP Core finds applications across diverse sectors, endorsed by major chip vendors

Deliverables

- ➔ Synthesizable RTL design in VHDL
- ➔ Easy-to-use UVM based verification environment
- ➔ Synthesis & Verification Scripts
- ➔ Technical documents